REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 37-41 and 48-52.

The Examiner also objected to certain claims as being duplicates. For example, the Examiner has taken the position that dependent Claim 34 is a substantial duplicate of dependent Claim 23. Each of these claims is dependent from different independent claims; Claim 34 is dependent from independent device Claim 32 and Claim 23 is dependent from independent method Claim 22. Consequently, since the independent claims are not duplicates, then the dependent claims, which include yet further distinguishing features of the invention, do not result in claim duplications.

The arguments supporting patentability of the claims are presented in detail below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 22, 32 and 43 over the Stolan patent. The present invention, as recited in independent Claim 32, for example, is directed to a watchdog timer for a microcontroller that generates refresh commands for the watchdog timer. The refresh commands are separated by a time interval within a predetermined range.

The watchdog timer comprises a refresh counter comprising a refresh input for receiving the refresh commands from the microcontroller. The refresh counter starts a refresh countdown on each receipt of a refresh command at the

refresh input, and generates a refresh command on expiration of the refresh countdown. A reset counter comprises a refresh input and a reset output. The reset counter starts a reset countdown on receipt of the refresh command generated by the refresh counter, and generates a microcontroller reset command at the reset output when the reset countdown times out.

The present invention may advantageously generate a microcontroller reset command even when the time interval separating successive refresh commands from the microcontroller is shorter than a minimum time period for normal operation, i.e., the refresh commands are generated repeatedly at too fast a rate. In other words, a time period between two successive refresh commands may be measured to determine if a reset command is to be generated.

Independent method Claim 22 is similar to independent device Claim 32. Independent device Claim 43 is directed to an electronic circuit comprising a microcontroller and a watchdog timer connected thereto. The watchdog timer is similar to the watchdog timer in independent device Claim 32.

Referring now to the Stolan patent, and in particular to FIG. 1, a selectively enabled watchdog timer circuit **10** receives periodic command signals (i.e., refresh commands) from a microcontroller **12**. In particular, the watchdog timer circuit **10** includes a cyclic counter **18** with an overflow bit for counting pulses provided by a timer **14**. The counter **18** alternately increments and decrements an output counter response to the periodic command signal from the microcontroller **12**. The failure of the microcontroller **12** to provide this command signal causes the counter to set the overflow bit, which resets the microcontroller. The Examiner

has interpreted the overflow bit as starting a refresh countdown on each receipt of a refresh command by the watchdog timer circuit **10**. The Examiner has taken the position that the Stolan patent discloses starting a refresh countdown on each receipt of a refresh command by the watchdog timer circuit **10**.

The Examiner acknowledges that Stolan does not explicitly disclose starting a reset countdown if the refresh command has timed out, and if the refresh command has not timed out when a next refresh command is received, then the reset countdown is not restarted. The Examiner states that the overflow bit is continuously set as the counter cycles through its maximum count as long as the microcontroller fails to provide the command signal. The Examiner has taken the position that it would have been obvious to start a reset countdown if the refresh countdown has timed out since Stolan teaches that the counter **18** cycles through its maximum count as long as the microcontroller **12** fails to provide the command signal.

The Examiner also makes reference to the size of the counter **18** and frequency of the timer **14** being chosen so that the duration between reset pulses is both long enough to afford the microcontroller **12** adequate time to prohibit the reset. The Examiner states that it would have been obvious to one skilled in the art to prohibit restarting of the reset countdown.

The Applicants respectfully disagree. Stolan fails to disclose that the watchdog timer circuit **10** includes a refresh counter for starting a refresh countdown on each receipt of a refresh command. In other words, the watchdog

timer circuit **10** fails to measure a time period between two successive refresh signals.

Instead, the refresh command is a periodic command signal from the microcontoller **12** to the counter **18** for changing the direction of the counter. Since the microcontroller **12** generates the refresh command, which is a periodic signal, then any refresh countdown would be performed by the microcontroller **12** and not the counter **18**.

In sharp contrast, the watchdog timer as recited in independent Claim 32 generates a refresh command on expiration of the refresh countdown. This may allow the watchdog timer to generate a microcontroller reset command even when the time interval separating successive refresh commands from the microcontroller is shorter than a minimum time period for normal operation, i.e., the refresh commands are generated repeatedly at too fast a rate.

Stolan generates a microcontroller reset command signal when the microcontroller fails to continuously generate refresh signals. Without refresh signals inverting its counting direction, the counter in Stolan reaches a limit, which leads to generation of the microcontroller reset command. If the microcontroller in Stolan continuously generates refresh commands, the counter may be sequentially incremented and decremented around an intermediate value. Then the counter would never reach its limit and no microcontroller reset command would be generated.

Accordingly, it is submitted that independent Claim 32 is patentable over Stolan. Independent Claims 22 and 43 are similar to independent Claim 32. It is submitted that these independent claims are also patentable over Stolan. In

view of the patentability of independent Claims 22, 32 and 43, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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